RENESAS

Microcontrollers and MOSFETs for

Chassis Applications

ISO 26262
ASIL D

Renesas Electronics
www.renesas.eu

2014.11

Highest functional safety requirements

The P Series was developed by Renesas for applications requiring the highest functional safety levels (up to ASIL D). This is realized by the highly efficient on-chip diagnostic features such as redundant CPU subsystem with compare unit, built-in self-tests for logic and memories, and ECC protection for on-chip memories.
Compliance with the functional safety standard ISO 26262 was inherent during development and analyzed throughout the course of safety assessments to ensure ASIL D conformity.

Functional safety

Intrinsic safety vs. software-based safety

While conventional Microcontrollers (MCUs) require additional monitoring software to supervise their correct function, development with intrinsically safe MCUs, like RH850/P1M and RH850/P1x-C, completely reduces this design effort.
This has many advantages for the ECU maker:

Smaller code

ASIL D compliance requires a high diagnostic coverage to detect random faults. Conventional MCUs require very complex diagnostic software to achieve this level of cover. The integral safety architecture of Renesas' P Series MCUs provides such diagnostic functions in hardware. This means a significant simplification and reduction of the code size, resulting in smaller memory sizes and shorter TATs.

Performance

By migrating diagnostic functions from software to highly efficient integrated hardware peripherals, with improved test coverage, the CPU can focus on its main purpose: running the application system. The 32-bit RH850 core delivers up to 2.8 DMIPS/MHz which corresponds to up to 1344 DMIPS for a dual core device like RH850/P1x-C running at 240 MHz!

Shorter development cycles

For the ECU manufacturer, the implementation and assessment of the system level functional safety architecture is an extremely complex and time-consuming task. The MCU analysis is an especially challenging task as it is one of the most complex components of the system. For an ECU manufacturer, the MCUs internal structure and failure modes makes this even more complicated, simply down to the limited MCU knowledge. In effect, Renesas has taken care of the safety assessment of the P Series devices. This significantly reduces the ECU engineering workload and helps to shorten development time.

MCU design considerations

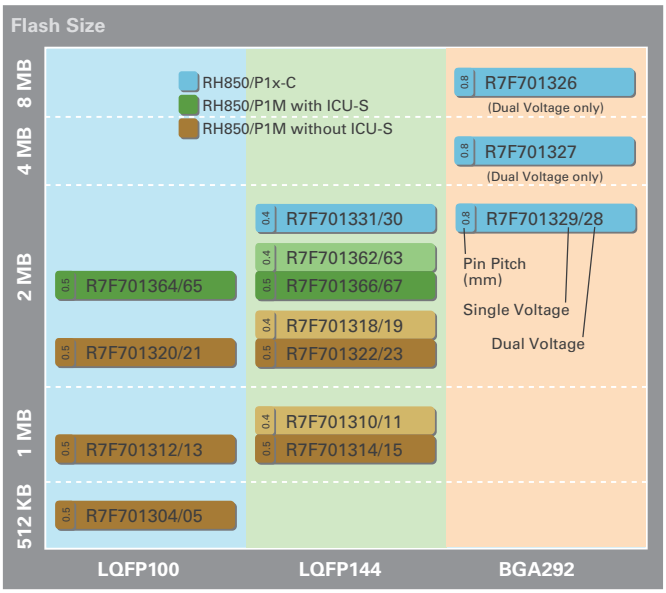
A detailed FMEA during the MCU design phase was used to identify relevant failure modes and to implement the appropriate diagnostics features in the hardware. This included fault scenarios that would not normally be covered by a conventional MCU or, if needed, only through high costs at the system level. The effectiveness of these diagnostic measures to meet ASIL D has been proven in special fault injection validations conducted during MCU development.

	V850E2/Px4	RH850/P1M	RH850/P1x-C
Number of Processor Elements (CPUs)	2 (In lock-step)	2 (In lock-step)	Up to 4 (2 x 2 in lock-step)
Code Flash	512 KB – 1 MB	512 KB – 2 MB	2 MB – 8 MB
Data Flash	32 KB	Up to 64 KB	Up to 224 KB
FlexRay™	2 ch.	Up to 2 ch.	Up to 4 ch.
SENT	–	6 ch.	Up to 8 ch.
PSI5	–	2 ch.	–
Cryptographic Unit	–	ICU-S (optional)	ICU-M (with 4 and 8 MB version)
ADC Channels	ADC 0: 22 ch.	ADC 0: up to 12 ch. ADC 1: up to 12 ch.	ADC 0: up to 20 ch. ADC 1: up to 20 ch.
Temperature Sensor	–	•	•
Max. Performance	Up to 410 DMIPS	448 DMIPS	Up to 1344 DMIPS
I/O Voltage	3.0 – 3.6 V or 4.5 – 5.5 V	3.0 – 5.5 V	3.0 – 3.6 V
Packages	LQFP144	LQFP100, LQFP144	LQFP144, BGA292

Feature comparison of microcontrollers for ASIL D applications

The next generation: RH850/P1M and RH850/P1x-C

RH850/P1M and RH850/P1x-C are the latest additions to Renesas' successful line of microcontrollers, targeting applications with functional safety requirements up to ASIL D. These devices are based on the proven V850E2/Px4 but feature a long list of improvements: significantly lower power consumption, more advanced on-chip peripherals, and more CPU performance just to name a few.



RH850/P1M and RH850/P1x-C product portfolio for ASIL D applications

Redundant CPU

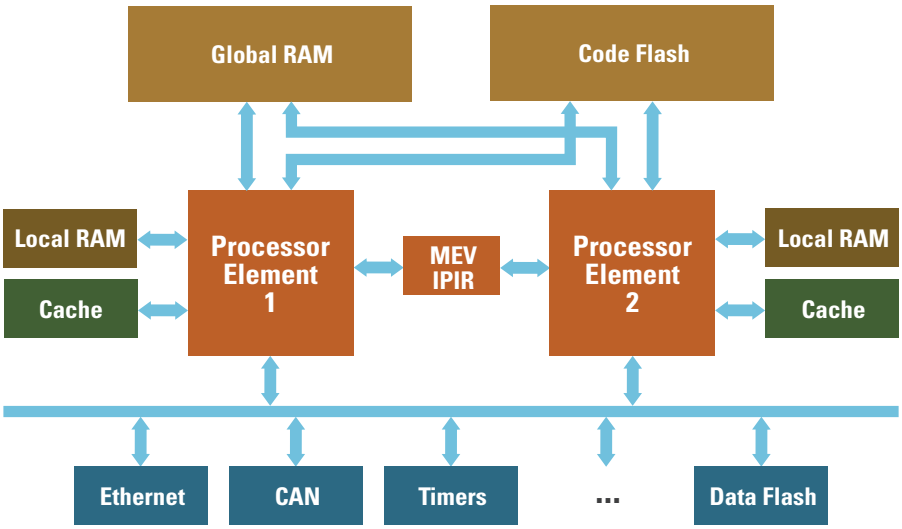
Redundancy of their most critical parts is key for systems with strong functional safety requirements. All RH850/P1x and RH850/P1x-C microcontrollers therefore incorporate for each Main Processor Element (with CPU, FPU, MPU, interrupt controller etc.) an identical Checker Processor Element. This executes in lock-step operation with two clock cycles delay exactly the same code as the Processor Element. If the integrated comparator detects any difference between the outputs of the Main Processor Element and the Checker Processor Element, it automatically triggers the Error Control Module to initiate appropriate actions before the failure puts the functional safety of the ECU at risk.
The redundancy of the Processor Elements is completely transparent to software and does not need to be taken into account in the implementation of the application code.

Built-in self-test (BIST)

Safety can be achieved only if all integrated functions work properly. All P Series devices therefore feature a built-in self-test that checks all relevant digital on-chip units in a matter of milliseconds during start-up. This self-test includes all internal volatile memories as well as many logic functions. Moreover, soft-error-robust flip-flops and ECC/EDC on all internal memories mitigate the occurrence of transient faults.

Dual core performance (RH850/P1H-C only)

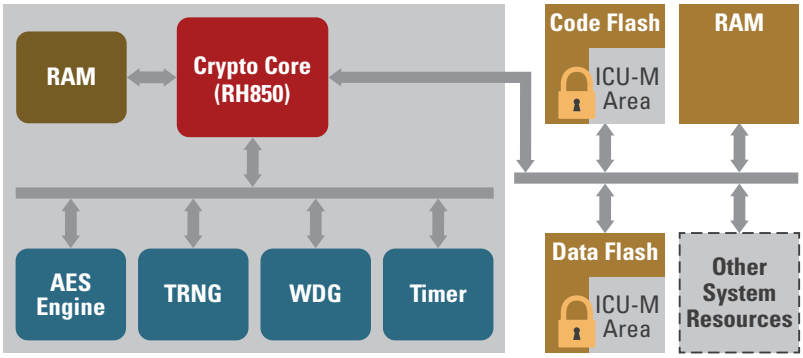
The more functions ECUs have to fulfil, the more performance is needed. RH850/P1x-C devices with 4 and 8 MB code flash incorporate two Processor Elements (PEs) and two Checker Processor Elements. The two Processor Elements deliver up to 672 DMIPS each or 1344 DMIPS in total. Both Processor Elements are identical and can access all peripherals. This means the ECU designer can achieve maximum flexibility regarding the partitioning of his software. For example, it is possible to run AUTOSAR non-time critical tasks on one Processor Element, while simultaneously executing time critical tasks on the second Processor Element (in a real-time operating system).
The inter-processor communication and semaphore handling between the two Processor Elements is supported by 34 dedicated 32-bit registers (MEV, IPIR) which are accessible by both Processor Elements.



Simplified block diagram of dual core RH850/P1H-C microcontroller (ICU-M not shown)

Data flash

All RH850/P1M and RH850/P1x-C devices feature dedicated data flash for storing non-volatile information (E²PROM emulation). Each 4-byte unit can be written more than 250,000 times. For security reasons, devices featuring an Intelligent Cryptographic Unit (ICU) offer an extra area of up to 32 KB for storing confidential information. The access to this area is limited to the ICU.
As code flash and data flash are separate blocks, the execution of application code does not interfere with write/ erase operations on data flash (dual operation).



Intelligent Cryptographic Unit M (ICU-M) for advanced cryptographic requirements like public key cryptography

Data-CRC peripheral

Functional safety on system level strongly depends on error-free transmission of information between the components of the system. The protection of data stream integrity by CRC checksums is therefore standard in such kind of systems.
In RH850/P1M and RH850/P1x-C, the calculation and verification of CRC checksums on data streams of arbitrary length is supported by up to eight dedicated hardware CRC units. The CRC polynomial can be selected for 32-bit Ethernet, 16-bit CCITT, 8-bit SAE J1850 or 8-bit 0x2F. As calculation is implemented in hardware, it has no impact on the CPU load.

Error control module

The ECM module collects error signals from various sources and monitoring systems. It also defines the action to be carried out upon the detection of a failure: signaling it at the ERROROUT pin, triggering an interrupt, or initiating a reset. A dedicated Error Delay Timer optionally allows the execution of program code before a failure is signaled to external components via the ERROROUT pin. This allows the MCU to be prepared for system shut-downs by external components.

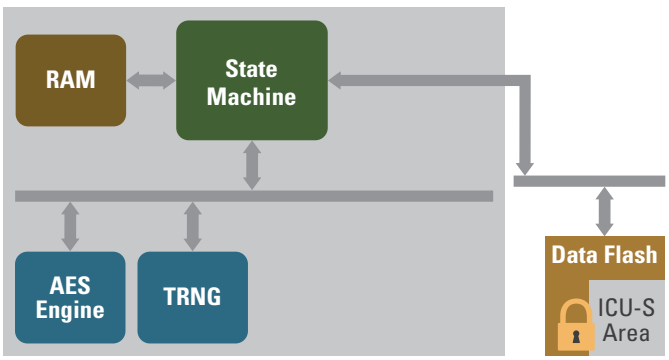
Intelligent Cryptographic Unit ICU-M (RH850/P1x-C only)

The ICU-M security module incorporates everything necessary to implement user-defined security services, from secure boot to autonomous memory check during run-time, from fast encryption/decryption to RSA signature verification. The ICU-M operates on a fully featured 80 MHz RH850 CPU that processes the programmed services, and has access to all resources within the device (global RAM, flash, peripherals). Program code and data for ICU-M are stored within secured and exclusive flash areas.

The ICU-M includes a powerful AES engine, which supports several complex block ciphers, including Galois/Counter mode (GCM) and XTS mode, with multiple execution contexts that can run in parallel. It also includes a true source of randomness. The Debugger Authentication Logic blocks malicious connection attempts from the outside and optionally disables any communication via CAN and FlexRay™ once an attack is detected.

Intelligent Cryptographic Unit ICU-S (RH850/P1M only)

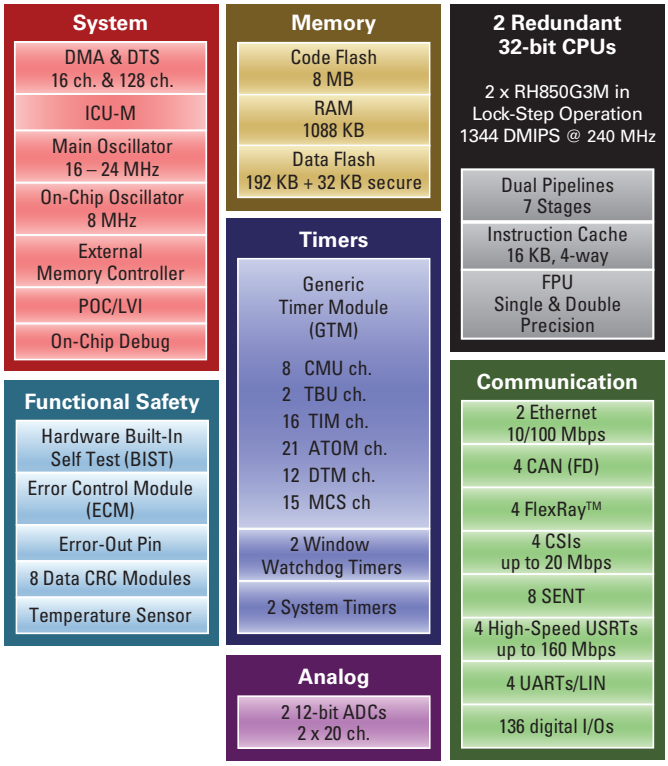
The optional SHE-compliant ICU-S security module provides an effective way to prevent software tampering and to secure CAN communications. It incorporates a state machine, protected RAM, an AES engine and a hardware random number generator (TRNG) that process the services as described in the SHE specification (encryption in ECB and CBC mode and CMAC generation and verification).
The ICU-S secret keys are stored in a protected data flash area, which is accessible only to the ICU-S and cannot be read or written by the main CPU.
RH850/P1M devices can be provided on request with a fixed, worldwide unique device ID. This can be used for example to control software updates or to unlock features only for individual ECUs.



Intelligent Cryptographic Unit S (ICU-S) for standard AES-128 encryption

Ethernet controller (RH850/P1x-C only)

RH850/P1x-C devices provide for 10/100 Mbps Ethernet connections an on-chip IEEE 802.3 conformant Media Access Controller (MAC) with up to two MII/RMII interfaces. To reduce CPU load, the controller supports automatic address filtering (except in promiscuous mode), CRC calculations and data transfer via DMA directly to RAM. The integrated magic package detection optionally triggers a Wake-on-LAN (WOL) interrupt which can be used for example to start the device.



Block diagram of dual core RH850/P1x

M-CAN (RH850/P1x-C only)

The M-CAN peripheral supports not only standard CAN as specified in ISO 11898-1 but also the CAN FD specification with a payload size of up to 64 bytes (instead of 8 bytes) and a maximum transmission rate of 8 Mbps (instead of 1 Mbps). This increases the CAN bandwidth significantly while compatibility is maintained.
The M-CAN of RH850/P1x-C also supports the TTCAN (time-triggered CAN) level 2 protocol according ISO 11898-4 in hardware.

RS-CAN (RH850/P1M only)

In contrast to previous device generations, the RS-CAN as implemented in RH850/P1x supports shared memory among multiple channels, flexible sizes of the used memory areas, and consequent assignment of FIFO structures. Thanks to this, a channel that needs more data and filter resources can take advantage of another channel needing less of these resources. The RS-CAN allows for diagnostic purposes to mirror all CAN messages to one CAN port. The CAN transfer layer fulfills all requirements defined in ISO 11898, SAE J1939 and CAN 2.0B standard.

FlexRay™

The optional FlexRay™ interface supports two communication channels up to 10 Mbps and is conformance tested to FlexRay™ protocol specification V2.1.

Key features

- 8 KB RAM, configurable from 30 message buffers with 254-byte data field each up to 128 message buffers with 48-byte data field each
- Fast CPU access to message buffers via I/O buffer
- Filtering by frame ID, channel ID or cycle number
- High clock accuracy
- Network management support

Feature	V850E2/Px4	RH850/P1M	RH850/P1x-C
Extended Safety Analysis on Peripherals	–	•	•
Checker Core delayed by two Clock Cycles	•	•	•
Optional Delay for ERROROUT Pin	–	•	•
Bus Protection	–	Parity	ECC
ECC on RAM and Code Flash	•	•	•
ECC on Data Flash	–	•	•
CRC Modules	2	4	up to 8
Error Injection Points	–	•	•
On-chip Temperature Sensor	–	•	•
Core Voltage Monitor (CVM)	–	•	•
WDT with changing Restart Code	–	•	•

Functional safety feature overview

A/D converters

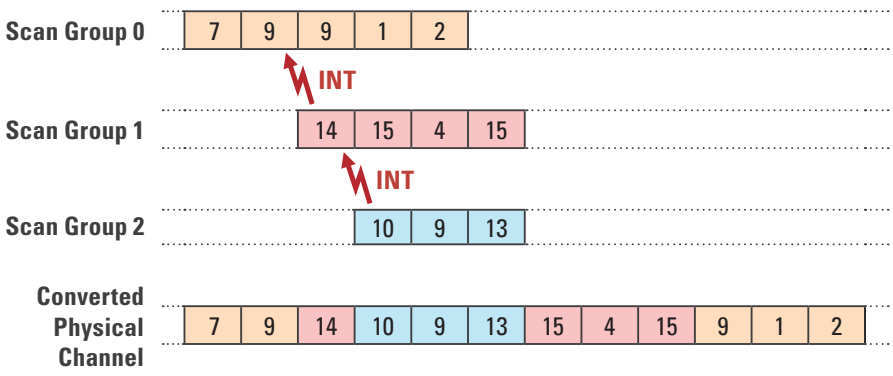
The integrated ADCs allow conversion with 12-bit resolution and a minimum conversion time of 1 µs. The assignment of analogue inputs to up to 72 Virtual ADC Channels in 10 Scan Groups allows to define complex conversion sequences with arbitrary priorities. These conversion sequences are processed autonomously by the ADC which stores the converted values into the Virtual Channel's result register.

In RH850/P1M, additional track-and-hold stages enable simultaneous snapshots of up to 10 analog signals that can then be converted successively. The correct function of the ADC is checked by an integrated self-test that performs manifold systematic tests of the complete signal path from the analog input pin via the external sample capacitors and the channel multiplexers to the actual A/D conversion unit.

Motor control & encoder timers (RH850/P1M only)

Each motor control timer can generate autonomously six center- or edge-aligned 16-bit PWM signals for the control of asynchronous and synchronous AC motors. Brushless DC (BLDC) motors can be controlled by 120° excitation mode that takes into account the inputs of three Hall sensors. Interconnections with other peripherals support enhanced functions like automatic calculation of the rotor position from Hall sensor signals, speed detection or A/D conversion triggering. For safety reasons, emergency shut-off is controlled by hardware and independent from any software. In addition to this, all RH850/P1M devices incorporate two dedicated encoder timers for the autonomous calculation of rotor positions of AC and BLDC motors based on rotary encoder signals (for BLDC in combination with the motor control timers and Hall sensors).

Virtual Channel	Physical Channel	Scan Group
0	7	0
1	9	0
2	9	0
3	1	0
4	2	0
5	14	1
6	15	1
7	4	1
8	15	1
9	10	2
10	9	2
11	13	2
...	...	...



Example for the usage of virtual ADC channels and scan groups.
The conversion results are stored for each virtual channel in a dedicated result register.

Generic Timer Module (RH850/P1x-C only)

The GTM is a very powerful and complex timer module which is capable to fulfill even the most sophisticated timer requirements.

It integrates a whole bunch of functional sub-modules, like Multi-Channel Sequencers (MCSs), Clock Management Units (CMUs), Time Base Units (TBUs), Timer Input Modules (TIMs), and Timer Output Modules (ATOMs). All these units are connected via the central Advanced Routing Unit (ARU). Each of the up to fifteen Multi-Channel Sequencers (MCSs) operates as a freely programmable, Turing complete CPU system for the processing of timer inputs and controlling of timer outputs. Dedicated Dead Time Modules (DTMs) support the generation of inverse signals, like it is necessary for the control of half bridges, in hardware.

Temperature sensor

All devices feature a temperature sensor to measure the junction temperature in single-shot or continuous mode. It can be configured to send an automatic notification to the Error Control Module (ECM) if an upper or lower limit is exceeded. In addition to this, the temperature sensor in RH850/P1x-C can optionally trigger an interrupt when the temperature rises or falls into one of two definable temperature ranges (high temperature range and standard operation temperature range).

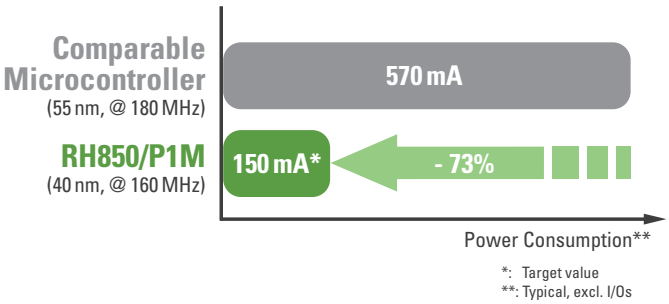
On-chip debugging

All RH850/P1M and RH850/P1x-C devices provide on-chip debugging via Nexus JTAG and Low Pin Debug (LPD) interface. In both cases, the debugger unit can be connected to the device without interrupting its operation (hot plugging) and can be used also to program the device's internal code and data flash.

For RH850/P1x-C, a special version of the microcontroller with even more debugging features is offered: RH850/PH1-CE. This device incorporates in addition to the debugging options of RH850/P1x-H a high-speed Nexus Aurora interface for collecting trace information in real-time. Like RH850/P1x, it also provides an AUD (Advanced User Debugger) monitor to access RAM, registers, code and data flash during runtime. All RH850/P1M and RH850/P1H-CE devices feature up to 2 MB dedicated Emulation RAM. This Emulation RAM can be mapped into the memory space of the code flash, virtually replacing its content. The content of the Emulation RAM can be modified via debug interface or by the microcontroller itself.

Extremely low power consumption

Thanks to the 40-nm process, the power consumption of RH850/P1M and RH850/P1x-C devices could be reduced significantly from previous generations and hence sets new standards for microcontrollers for ASIL D applications. This opens the door for costs savings in several parts of the ECU, like in the power supply circuitry. The much lower power dissipation of this new generation of functional safety microcontrollers also invites to evaluate new, previously impossible heat sink solutions.



RH850/P1M consumes only about ¼ of the current other, comparable microcontrollers need.

Tools

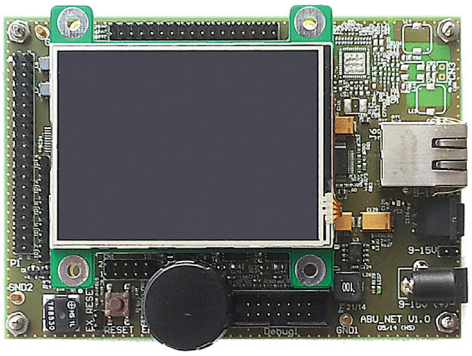
RH850/P1x-C starter kit

Y-ASK-RH850P1X-C

This starter kit comes with everything necessary for a fast and smooth start with RH850/P1x-C. The board itself is fully equipped with

- RH850/P1x-C microcontroller with 4 MB on-board flash
- 2.7" colour TFT (320 x 240) with touch panel
- 2 Ethernet interfaces (RJ45 & Broadcom BroadR-Reach®)
- 3 CAN/CAN FD, 2 RS232, 3 LIN, 2 FlexRay™, CSI, I/O interfaces
- Rotary encoder with push-button, buzzer
- ICs for power consumption measurement (1.25 V and 3.3 V)
- Connector for E1 on-chip debugger

The package includes besides the board the E1 on-chip debugger, a power supply, a 90-day evaluation version of Green Hills' Multi IDE, and a CD-ROM with documentation and sample code.

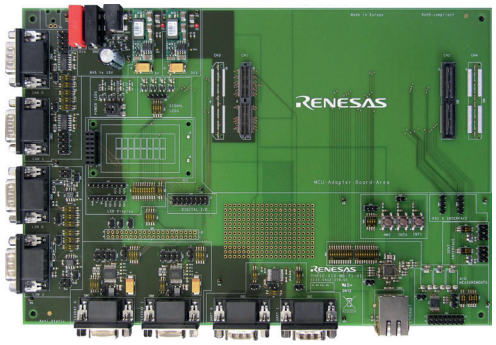


Board dimensions: 330 mm x 187 mm

RH850 evaluation platform main board Y-RH850-X1X-MB-T1-V1

This generic board for RH850 software development hosts device-specific Adapter Boards and provides a large set of peripherals:

- Various interfaces/connectors:
  – 2 CAN, 2 LIN
  – FlexRay™ (2 channels)
  – Ethernet
  – 2 UART/RS232, 2 SENT, 2 PSI5
- 4 signal LEDs (active high), 3 push buttons, 3 analogue inputs
- LCD module, breadboard area



Board dimensions: 260 mm x 174 mm

The package includes a CD-ROM with user's manual and schematic.

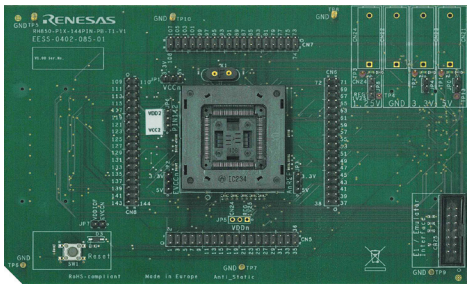
Functional safety microcontroller portfolio with RH850/P1M and RH850/P1x-C

Group	Part Number	Main CPU(s)	Clock Frequency	Code Flash	Data Flash	RAM	Emulation RAM	CAN	Ethernet	FlexRay™
RH850/P1M	R7F701304	RH850	160 MHz	512 KB	32 KB	64 KB	8 KB	2 ch. (CAN)	–	–
	R7F701305									
	R7F701312			1 MB		128 KB				
	R7F701313									
	R7F701310									
	R7F701311									
	R7F701314									
	R7F701315									
	R7F701320			2 MB	64 KB		32 KB	3 ch. (CAN)		2 ch.
	R7F701364									
	R7F701321									
	R7F701365									
	R7F701318									
	R7F701362									
	R7F701319									
	R7F701363									
	R7F701322									
	R7F701366									
	R7F701323									
	R7F701367									
RH850/P1M-C	R7F701331	RH850	240 MHz	2 MB	96 KB	448 KB	–	3 ch. (CAN FD)	1 ch.	2 ch.
	R7F701330									
	R7F701329									
	R7F701328									
RH850/P1H-C	R7F701327	2 x RH850	2 x 240 MHz	4 MB	160 KB	1088 KB			2 ch.	4 ch.
	R7F701326			8 MB	192 KB			4 ch. (CAN FD)		
RH850/P1H-CE	R7F701325			10 MB		1536 KB	2 MB			

RH850 evaluation platform adapter boards

Y-RH850-P1X-100PIN-PB-T1-V1 (LQFP100, 0.5 mm p. p.)
Y-RH850-P1X-144PIN-PB-T1-V1 (LQFP144, 0.4 mm p. p.)
Y-RH850-P1X-C-144PIN-PB-T1-V1 (LQFP144, 0.4 mm p. p.)
Y-RH850-P1X-C-292PIN-PB-T1-V1 (BGA292)
Y-RH850-P1X-C-404PIN-PB-T1-V1 (BGA404)

Adapter Boards can be operated plugged into the RH850/x1x Evaluation Platform Main Board or stand-alone. They are equipped with an E1 connector and a test socket to hold RH850/P1M devices (not included).

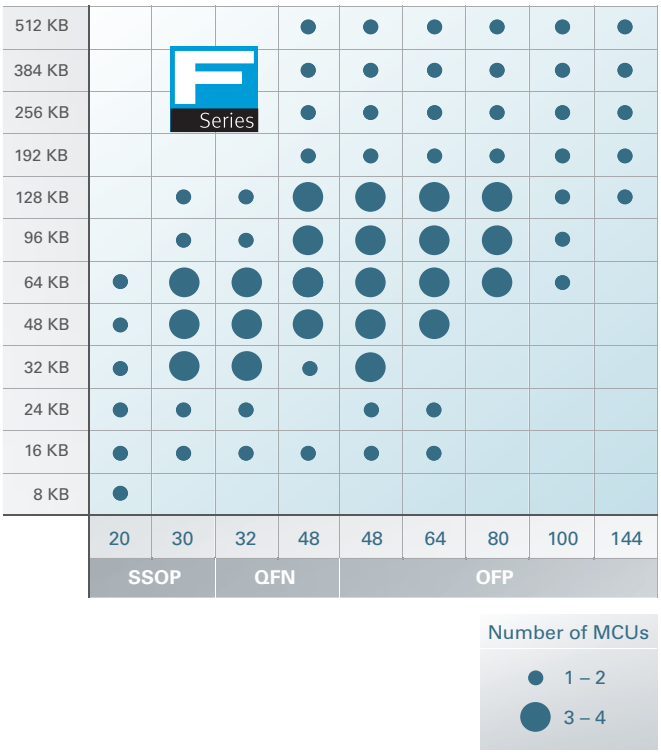


Board dimensions: 160 mm x 100 mm

ADC 0	ADC 1	CSIs/ USRTs	SENT	Crypto Unit	CRC Units	Approximate Performance	Supply Voltage	Supply Voltage (Core, I/Os)	Pin Count	Package Type
9 x 12-bit	10 x 12-bit	8	5 ch.	–	4	448 DMIPS	3.0 – 5.5 V	n/a	100	LQFP, 0.5 mm p. p.
								1.15 - 1.35 V		
								n/a		
								1.15 - 1.35 V		
12 x 12-bit	12 x 12-bit		6 ch.					n/a	144	LQFP, 0.4 mm p. p.
								1.15 - 1.35 V		
								n/a		LQFP, 0.5 mm p. p.
								1.15 - 1.35 V		
9 x 12-bit	10 x 12-bit		5 ch.	–				n/a	100	
				ICU-S						
				–				1.15 - 1.35 V		
				ICU-S						
12 x 12-bit	12 x 12-bit		6 ch.	–				n/a	144	LQFP, 0.4 mm p. p.
				ICU-S						
				–				1.15 - 1.35 V		
				ICU-S						
				–				n/a		LQFP, 0.5 mm p. p.
				ICU-S						
				–				1.15 - 1.35 V		
				ICU-S						
12 x 12-bit	8 x 12-bit	6	6 ch.	ICU-M	4	672 DMIPS	3.0 – 3.6 V	n/a	144	LQFP, 0.4 mm p. p.
								1.15 - 1.35 V		
12 x 12-bit	12 x 12-bit							n/a	292	BGA, 0.8 mm b. p.
								1.15 - 1.35 V		
16 x 12-bit	16 x 12-bit	8	8 ch.		8	1344 DMIPS				
20 x 12-bit	20 x 12-bit		10 ch.						404	

16-bit Microcontroller RL78/F1x

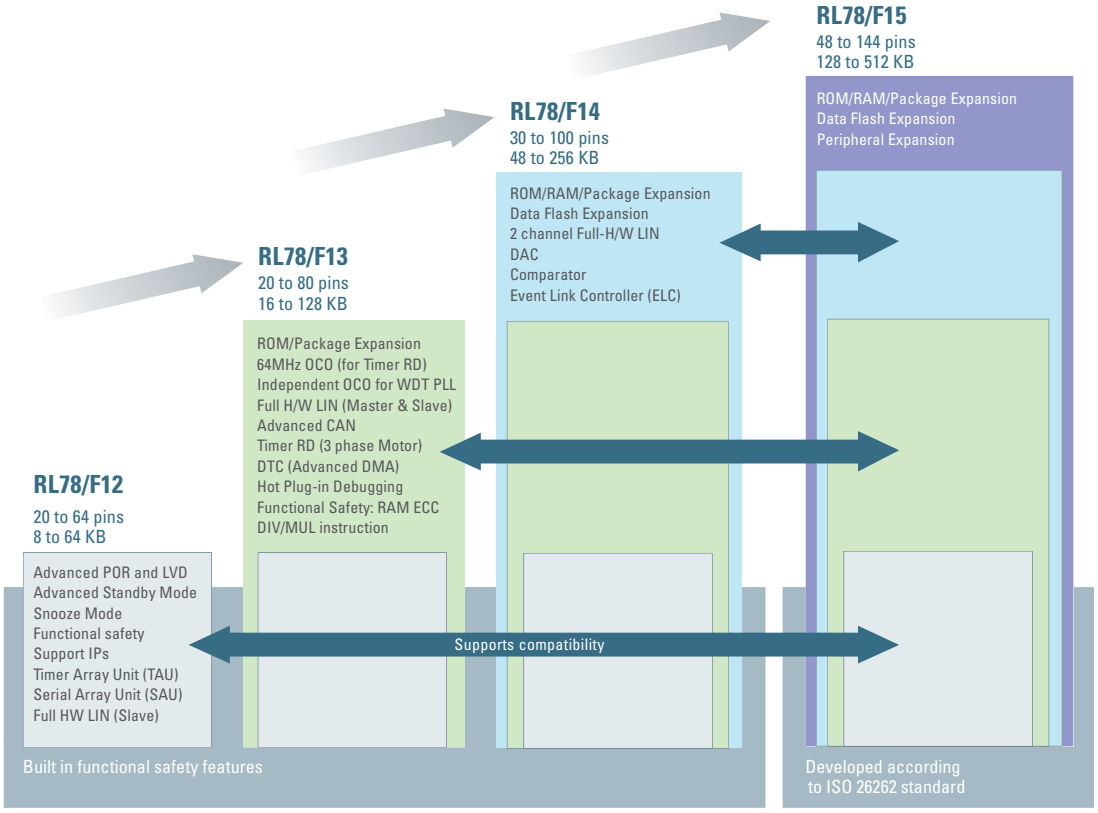
- 16-Bit device technology shrunk to 130 nm
- Huge scalability with more than 120 derivatives
- Many new energy saving features integrated
- Ultra low power consumption
  - Reduced to 50% compared to previous generation
  - RUN mode: typ. 0.2 mA/MHz and max. 0.4 m A/MHz
- Strong performance CPU with 1.6 DMIPS/MHz
- Increased ambient temperature of up to 150 °C
- Improved Data Flash memory with minimum 100,000 write/erase cycles
- High integration enabling system cost reduction
  - High precision on chip oscillator (+/- 2% at -40 to 105 °C) fully suitable for LIN
  - 64 MHz on-chip high-speed clock for dedicated peripherals



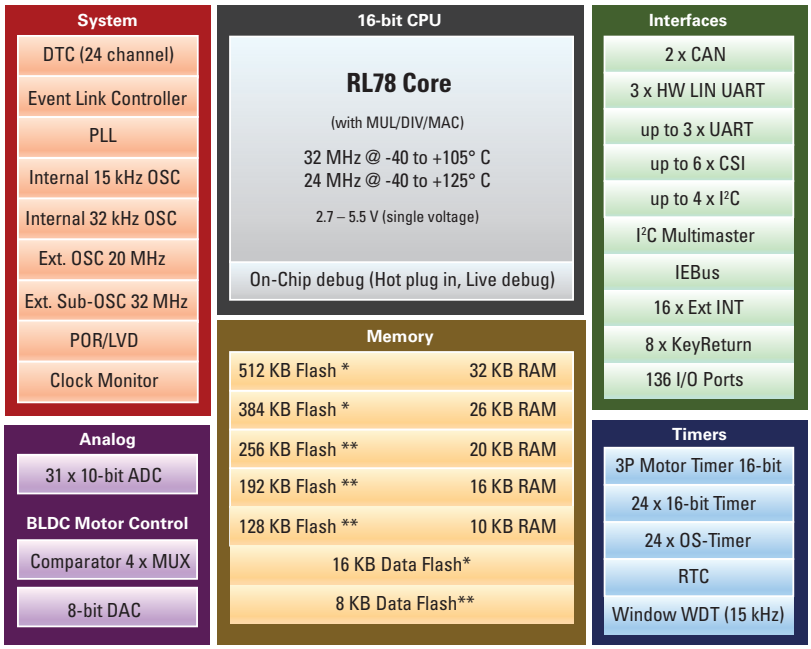
Device concept

Basis of the concept is the compatibility. That supports the flexibility during the design of the application to move to amore suitable derivative in case of significant changes.

The portfolio of the RL78/F1x is the largest among all 16-bit MCU suppliers.



Block diagram RL78/F15 – 144-pin QFP



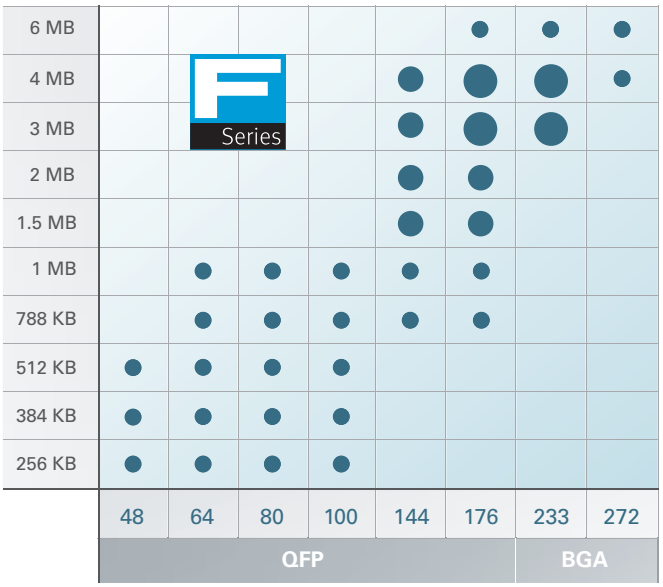
RL78/F1x feature line-up

		16-bit			
		RL78/			
		F12	F13	F14	F15
Basics	Flash	8 – 64 KB	16 – 128 KB	48 – 256 KB	128 – 512 KB
	RAM	0.5 – 4 KB	1 – 8 KB	4 – 20 KB	10 – 32 KB
	Data flash	4 KB	4 KB	4 – 8 KB	8 – 16 KB
	Package pins/balls	20 – 64	20 – 80	30 – 100	48 – 144
Peripherals	Ethernet	–	–	–	–
	FlexRay	–	–	–	–
	Security (cryptographic)	–	–	–	–
	CAN	–	0 – 1	1	2
	CAN FD™	–	–	–	–
	LIN	1	1	1 – 2	2 – 3
	UART	2 – 4	1 – 2	2	2 – 3
	CSI	2 – 7	2 – 4	3 – 4	4 – 6
	I²C	1 – 7	2 – 5	3 – 5	5
	ADC 10-bit	4 – 12	4 – 20	10 – 31	18 – 31
	ADC 12-bit	–	–	–	–
	PWM	4 – 7	7 – 16	11 – 20	15 – 27
	16-bit timer	9	17 – 21	21 – 25	25 – 33
	32-bit timer	–	–	–	–
Supply	Max. CPU clock	32 MHz	32 MHz	32 MHz	32 MHz
	Min. voltage	1.8 V	2.7 V	2.7 V	2.7 V
	Max. voltage	5.5 V	5.5 V	5.5 V	5.5 V
Temperature	Min. temperature	-40 °C	-40 °C	-40 °C	-40 °C
	Max. temperature	+125 °C	+150 °C	+150 °C	+125 °C
Support	AUTOSAR MCAL	–	–	–	–
	Functional safety	–	✓	✓	✓
	- FMEDA	–	✓	✓	✓
	- Design	–	–	–	✓
	- ASIL	–	–	–	B

32-Bit Microcontroller RH850/F1x

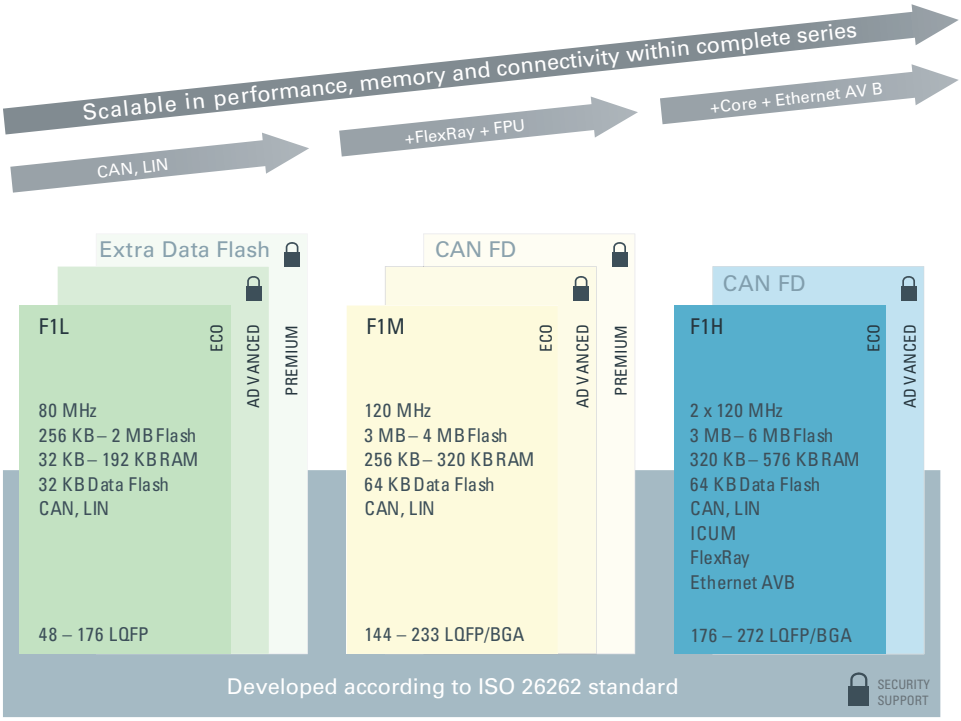
- 32-bit device technology shrunk to 40 nm
- Huge scalability with more than 80 derivatives
- Many new energy saving features integrated
- Super low power
  - RUN mode: typ. 0.3 mA/MHz and max. 0.75 mA/MHz
- High performance CPU with up to 3.04 DMIPS/MHz
- Ambient temperature up to 125 °C supported
- Improved Data Flash memory with minimum 125,000 write/erase cycles
- Full coverage of body networking interfaces supported
  - CAN, CAN FD, LIN
  - FlexRay™, Ethernet AVB

RENESAS RH850

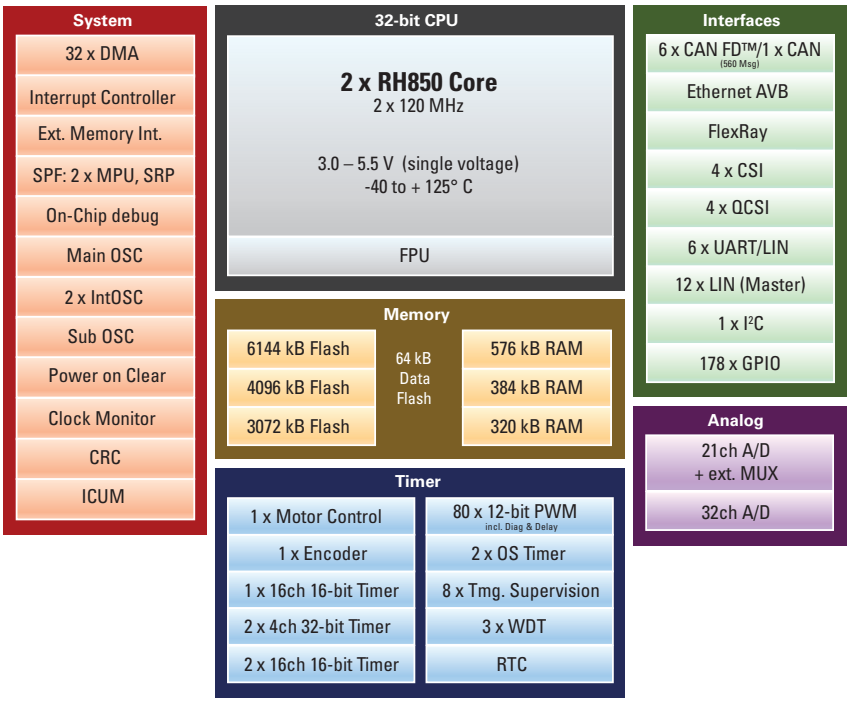


Device concept

The RH850 Family represents the next generation 32-bit RISC microcontroller to endorse future automotive applications. The F Series products, designed for body applications, provide high scalability, extreme low power consumption and a broad range of networking IPs.



Block Diagram RH850/F1H – 233-pin BGA



RH850/F1x feature line-up

		32-bit							
		RH850/							
		F1L			F1M			F1H	
		ECO	ADVANCED	PREMIUM	ECO	ADVANCED	PREMIUM	ECO	ADVANCED
Basics	Flash	256 – 2 MB	768 – 2 MB	1.5 – 2 MB	3 – 4 MB	3 – 4 MB	3 – 4 MB	3 – 6 MB	3 – 4 MB
	RAM	32 KB	32 KB	64 KB	256 – 320 KB	256 – 320 KB	256 – 320 KB	320 – 736 KB	256 – 320 KB
	Data flash	32 KB	32 KB	46 KB	64 KB	64 KB	64 KB	64 KB	64 KB
	Package pins/balls	48 – 176	64 – 176	144 – 176	144 – 233	144 – 233	144 – 233	176 – 272	144 – 233
Peripherals	Ethernet	–	–	–	–	–	–	✓	✓
	FlexRay	–	–	–	✓	✓	✓	✓	✓
	Security (cryptographic)	–	✓	✓	✓	✓	✓	✓	✓
	CAN	1 – 6	1 – 6	1 – 6	6	6	6	7 – 8	7
	CAN FD™	–	–	–	–	–	6	–	6
	LIN	3 – 16	3 – 16	3 – 16	12 – 16	12 – 16	12 – 16	12 – 18	12 – 18
	UART	1 – 6	1 – 6	1 – 6	6	6	6	2 – 6	6
	CSI	2 – 6	2 – 6	2 – 6	6	6	6	6 – 8	8
	I²C	1	1	1	1	1	1	1	1
	ADC 10-bit	4 – 28	4 – 28	4 – 28	22 – 34	22 – 34	22 – 34	26 – 38	26 – 38
	ADC 12-bit	8 – 32	8 – 32	8 – 32	24	24	24	32	32
	PWM	13 – 72	13 – 72	13 – 72	64 – 80	64 – 80	64 – 80	40 – 96	72 – 80
	16-bit timer	16 – 48	16 – 48	16 – 48	21 – 48	21 – 48	32 – 48	32 – 48	48
	32-bit timer	5 – 9	5 – 9	5 – 9	13	13	13	18	18
Supply	Max. CPU clock	80 MHz	96 MHz	96 MHz	120 MHz	120 MHz	120 MHz	2 x 120 MHz	2 x 120 MHz
	Min. voltage	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V
	Max. voltage	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V
Temperature	Min. temperature	-40 °C	-40 °C	-40 °C	-40 °C	-40 °C	-40 °C	-40 °C	-40 °C
	Max. temperature	+125°C	+125 °C	+120 °C	+125 °C	+125 °C	+125 °C	+125 °C	+125 °C
Support	AUTOSAR MCAL	✓	✓	✓	✓	✓	✓	✓	✓
	Functional safety	✓	✓	✓	✓	✓	✓	✓	✓
	- FMEDA	✓	✓	✓	✓	✓	✓	✓	✓
	- Design	✓	✓	✓	✓	✓	✓	✓	✓
	- ASIL	B	B	B	B	B	B	B	B

Complete MCAL packages

Since the early days of AUTOSAR, Renesas provides AUTOSAR Release 3 Microcontroller Abstraction Layer (MCAL) for Renesas 32-bit microcontrollers. Meanwhile, Renesas has expanded its roadmap to incorporate AUTOSAR Release 4 compliant drivers, which support automotive Ethernet and safety relevant solutions.

Support

Together with the actual MCAL software licenses, Renesas offers a whole set of MCAL related services including: support & maintenance, engineering services, customizations and, last but not least, customer training. All these AUTOSAR activities are coordinated in Europe by the AUTOSAR Software Competence Centre, located in Düsseldorf, Germany.

License models

Renesas offers MCALs in three different license models to meet different requirements:

Development

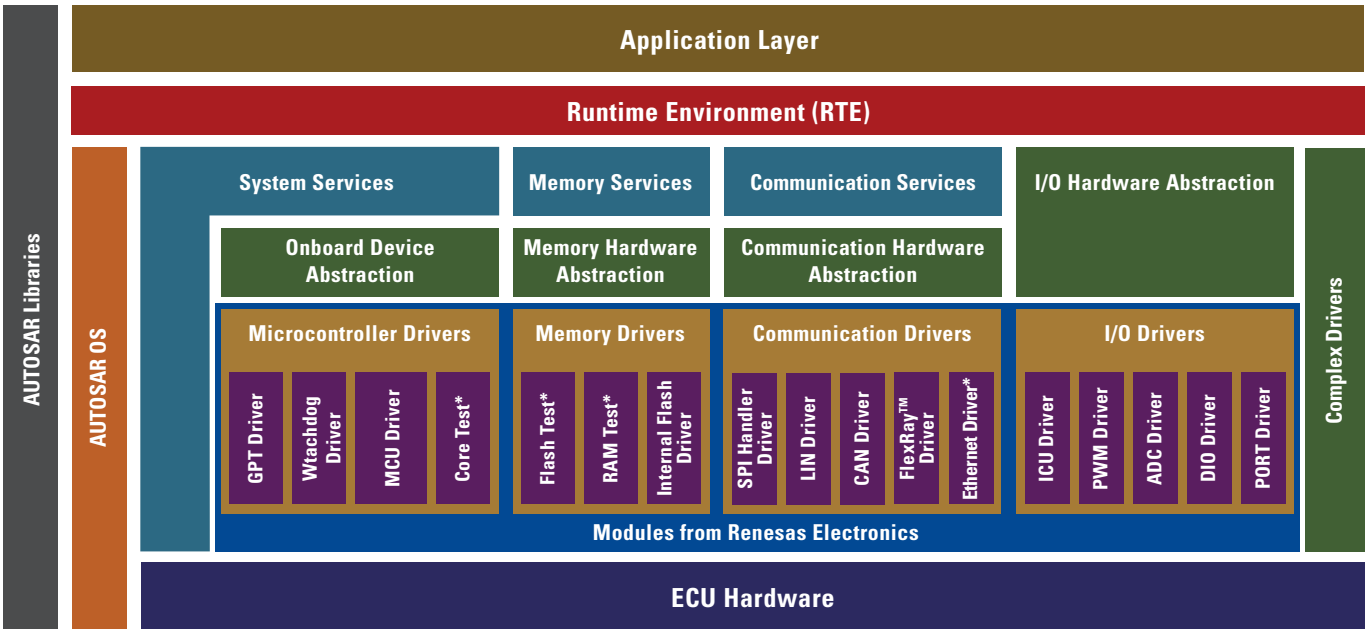
This license type is for MCAL evaluation, development and prototyping purposes for a period of 12 months.

Single-project

This license type entitles the licensee to use an MCAL for one specified project.

Multi-project

This is the preferred license type if an MCAL is required for several projects.



*Only in AUTOSAR Release 4

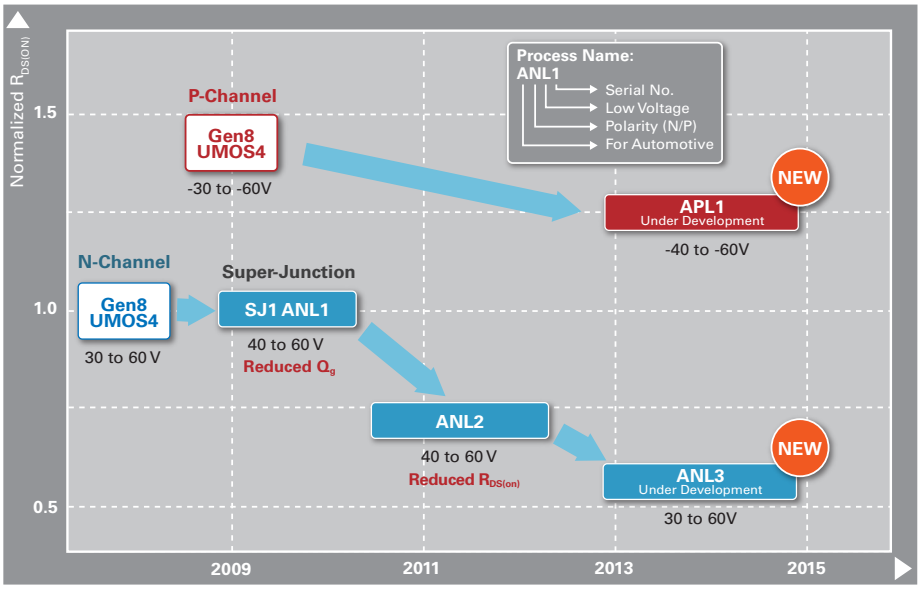
AUTOSAR basic software modules including Microcontroller Abstraction Layer (MCAL)

PowerMOSFETs

Chassis applications need the whole portfolio of low-voltage PowerMOSFETs, from power devices in small packages for ABS/ESP systems to high-power packages as well as bare dies for EPS. Renesas offers advanced silicon technologies, reliable packages and known good dies (KGDs) to meet any or all of these requirements.

Technology

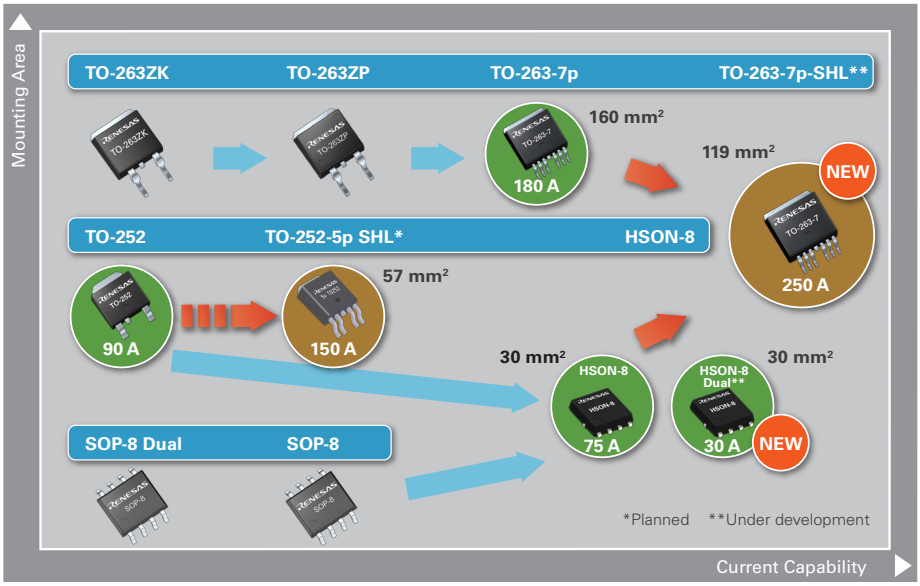
Advanced silicon technologies are the key success factor for offering superior PowerMOSFETs. Renesas' ANL2 N-channel technology significantly reduces $R_{DS(ON)}$ and gate charge Q_G compared with the latest well known UMOS-4 trench technology. Accordingly switching losses and on-losses are drastically reduced – ideal for high power switching applications. With its outstanding FOM performance ($R_{DS(ON)}$ x Q_G), this technology will considerably increase the efficiency of modern chassis applications. ANL2 PowerMOSFETs and its broad line-up cover the performance requirements of a wide range of chassis applications.



$R_{DS(ON)}$ reduction by optimized trench structures

Packages

PowerMOSFETs come in highly reliable standard packages like DPAK and D2PAK, but Renesas also offers new packages with improved electrical and thermal characteristics for automotive applications. D2PAK-7-pin increases current capability up to 180 A and reduces the package resistance – it's the obvious choice for high-performance applications. To support further mounting area reduction requirements, advanced versions of the DPAK and D2PAK-7-pin packages with reduced footprint are being developed by introducing shorter head and leads (SHL). In the field of small packages the HSON-8 combines the small size of SOP-8 footprint with performance and reliability comparable to that of DPAK and standard packages – the best solution for all space-constrained applications.



PowerMOSFET package roadmap

All automotive PowerMOSFETs are qualified to AEC-Q101; 175 °C rated and comply with RoHS and ELV directives.

Download this brochure at
www.renesas.eu/chassis_brochure

Before purchasing or using any Renesas Electronics products listed herein, please refer to the latest product manual and/or data sheet in advance.

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